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REMARKS/ARGUMENTS

Reconsideration is requested in view of the following remarks. Claim 7 has been editorially revised. Support for this revision can be found on page 18, lines 30-34 of the specification, among other places. The limitation added to claim 7 was presented previously in claim 21. Claims 7-20 remain pending in the application, with dependent claims 9-15 and 18-20 being withdrawn.

Claim Rejections – 35 USC §102

Claim 7 is rejected under 35 U.S.C. §102(e) as anticipated by DeBoer et al. (US 6,737,696). Applicant respectfully traverses this rejection. This rejection is moot since claim 21 was not rejected under 35 U.S.C. §102.

Claim Rejections – 35 USC §103

Claims 7-8, 16-17 and 21 are rejected as unpatentable over Huang (US 6,617,631) in view of DeBoer et al. Applicant respectfully traverses this rejection.

Claim 7 is directed to a method of manufacturing a semiconductor memory device wherein the length of a portion where the opposing capacitors are overlapped in the mask layout is set so that the value of the parasitic capacitance between adjacent cell capacitors is not more than 10% of the set cell capacitance value. This feature reduces parasitic capacitance between adjacent cell capacitors to suppress malfunctions caused by noise without changing the conventional capacitor shape, capacitance, or the like.

DeBoer et al. are directed to a capacitor structure like that shown in Figure 15 of the specification. The capacitor structure disclosed by DeBoer et al. is therefore different from the structure recited in claim 7 because parasitic capacitance is not caused between adjacent cell capacitors in the capacitor structure disclosed by DeBoer et al. as discussed from page 3, line 2 to page 4, line 12 of the specification. The adjacent cell capacitors disclosed by DeBoer et al., for example, are connected electrically by a common plate electrode. Since the electric potential is the same everywhere along the common plate electrode, a large parasitic capacitance is not generated between the adjacent cell capacitors, even if the plate electrode is covered with an interlayer insulating film.

DeBoer et al. thus does not disclose the reduction of a parasitic capacitance or even suggest the feature of sufficiently reducing the parasitic capacitance such as recited in claim 7. Although DeBoer et al. disclose a stagger structure, DeBoer et al. do not teach or suggest that such a structure can be designed to reduce a parasitic capacitance.

Huang does not remedy the deficiencies of DeBoer et al. Neither Huang alone or in combination with DeBoer et al. teach or suggest that the length of a portion where the opposing capacitors are overlapped in the mask layout is set so that the value of the parasitic capacitance between adjacent cell capacitors is not more than 10% of the set cell capacitance value. For at least these reasons, claim 7 is patentable over DeBoer et al. alone, or in combination with Huang. Claims 8 and 16-17 are patentable over the cited art since they depend from claim 7 that is allowable. The features of claim 21 have been added to claim 7; and claim 21 has been canceled. Applicant does not concede the correctness of the rejection.

Favorable reconsideration in the form of a Notice of Allowance is requested. If the Examiner believes a telephone conference would advance the prosecution of this application, the Examiner is invited to telephone Applicant's primary attorney-of-record, Douglas P. Mueller (Reg. No. 30,300), at (612) 455-3804.

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Respectfully submitted,

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